SEMICONDUCTOR MEMORY CELL WITH BURIED DOPANT BIT LINES AND SALICIDED POLYSILICON WORD LINES ISOLATED BY AN ARRAY OF BLOCKS

ABSTRACT OF THE DISCLOSURE

A method for manufacturing ROM memory devices. The method includes forming a trench isolation structure within a cell region of a semiconductor substrate. The cell region is an array region for ROM memory devices. The method includes forming a gate structure within the cell region and forming a sidewall spacer on the gate structure, which is configured to overlap a portion of the trench isolation structure within the cell region to separate a buried bit line region of the cell region from an adjacent cell region. The method applies a refractory metal layer overlying the gate structure including sidewall spacers and exposed portion of the trench isolation structure. A step of alloying the refractory metal layer to the gate structure and exposed portions of source/drain regions to form silicided regions overlying the gate structure and source/drain regions is included. The refractory metal layer is selectively removed from sidewall spacers and exposed portion of the trench isolation structure.

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